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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,316	06/26/2003	Hong Wang	42P16547	8010

8791 7590 07/27/2006

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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,316	WANG ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-30 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6-7, 9-11, 14-15, are 17-19 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Park (Patent No. 6,988,190).

4. Note in relation to applicants' claims to "converting at least some of the instructions in a stream into ISA-implementation specific instructions", Park taught a decoded instruction trace cache which would have all of its instructions as ISA-implementation specific instructions (col. 4, lines 3-6).

5. Claims 1-2, 6-10, 14-18, 20-22, and 25-29 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Ramirez et al. (Fetching Instruction Streams).

6. The examiner would suggest applicants read Section 2.2, at a minimum, before responding.

7. Claims 1-2, 6-10, 14-18, 20-22, and 25-29 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Nair et al. (Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups).

8. Claims 1-2, 4-10, 12-18, 20-22, and 24-29 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Nair (Patent No. 6,304,962).

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 3, 11, 19, 23, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair (Patent No. 6,304,962).

12. In relation to applicants' claims to having a start instruction pointer and end instruction pointer (claims 3, 11, 19, 23, and 30) which depend from applicants' claims 1-2, 9-10, 17-18, 20-22, and 27-29, Nair taught the functional equivalent which is a start instruction pointer and length field which when combined yield the end instruction pointer (col. 4, lines 31-51).

13. Claims 7, 15, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair (Patent No. 6,304,962).

14. Nair speaks of his invention in relation to superscalar processors (col. 1, lines 24-33), and the examiner takes Official Notice that many such processors are based on RISC instruction sets that are directly decodable and therefore constitute ISA-implementation specific instructions used to make up the superblocks of Nair resulting in such instructions being contiguous with the blocks.

15. The drawings are objected to because Figure 1 has not been labeled "Prior Art" though applicants call it such in their specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

16. Applicant's arguments filed 5/2/2006 have been fully considered but they are not persuasive.

17. Applicants have argued on behalf of their claims: (a)"Claims 1, 9 and 17 include the elements of 'defining a plurality of streams based on the examining, wherein each stream comprises a sequence of basic blocks in which only a last block in the sequence ends in a branch instruction, the execution of which causes program flow to branch, the remaining basic blocks in the stream each ending in a branch instruction, the execution of which does not cause program flow to branch' (claim 1) or similar elements. Claims 20 and 27 include the elements of 'wherein the predicted stream comprises a sequence of basic blocks in which only a last block in the sequence ends in a branch instruction, the execution of which causes program flow to branch, the remaining basic blocks each ending in a branch instruction, the execution of which does not cause program flow to branch' (claim 20) or similar elements. The cited references do not teach defining such streams." and (b) "Also, Applicants believe that claims 7, 15 and 26, as amended, are not taught by the cited references. Specifically, the cited references do not teach storing an 'ISA-implementation specific instructions' in 'memory locations contiguous to the basic blocks.' If the Examiner maintains the rejection of any of these claims, the Applicants respectfully request that the Examiner particularly point out those sections of the cited references that teach each of these elements."

18. As to 14(a), Ramirez et al. (Fetching Instruction Streams) teaches multiple approaches which result in determining streams as applicant is claiming. Ramirez describes on page 373 the work of Yeh and Patt on a fetch engine which fetches basic blocks and their suggestion that "basic blocks should not be terminated at branches which have never been taken, that is, that only taken branches should introduce a basic block in the BTB" (i.e., the results of program execution seen at the writeback/commit stage of a processor enable the fetch engine to determine/establish instruction streams). Ramirez also describes work by Reinman, Austin, and Calder (p. 373) who teach a Fetch Target Buffer (FTB) with variable length fetch blocks where a fetch block is defined as a sequence of instructions starting at a branch target, and ending at a strongly biased taken branch with strongly biased not-taken branches embedded therein (i.e., the results of program execution seen at the writeback/commit stage of a processor enable their system to determine/establish instruction streams). Ramirez also describes trace caches (pp. 373-374) such as the micro-op trace cache of the Pentium 4 produced by applicants' assignee which would inherently provide, over time, a plurality of streams as applicants have claimed as well as functional equivalents of such streams in that there would be streams of instructions with multiple internal branches which do not branch outside of the stream. The results of program execution seen at the writeback/commit stage of a processor enable trace cache systems to establish instruction streams. Finally, Ramirez taught about his own research explains in the portion of the Introduction (p. 371) underlined by the examiner to assist applicants: "An instruction stream is a sequential run of instructions, from the target of a

taken branch, to the next taken branch (called a dynamic block in the literature). A single instruction stream may contain multiple basic blocks, and multiple branches, as long as all the intermediate branches are not taken." On page 372, Ramirez explains he determines steams by using profile data (i.e., he runs the program and looks at what is written-back/committed). Nair (Patent No. 6,304,962) taught streams in the form of superblocks where "A superblock is a set of instructions in consecutive address locations terminated by a branch that is known to have been taken." Nair (Patent No. 6,304,962) also specifically taught: "The following example describes the case when a misprediction is detected (upon resolution of a superblock). In the example, the number of entries in STB 404 and, thus, the number of exits for a particular superblock, is limited to 4. However, it is to be appreciated that the preceding scheme may be readily modified by anyone skilled in the art to include more or less than the 4 exits described in the corresponding example." In other words, Nair (Patent No. 6,304,962) taught final determination of streams/superblocks is done at writeback/commit time, and the number of exits of a superblock could be modified to be one exit by one of ordinary skill resulting in applicants' streams. Note also on at col. 9, lines 56-57, Nair is discussing intermediate branches within the superblock meaning intermediate blocks with branches which are not taken are present. Nair (Exploiting Instruction Level ...) describes the concept of a DIF group system which has the potential to produce applicants claimed streams and whose primary engine determines DIF groups (pp. 15 and 16). Park (Patent No. 6,988,190) taught a trace cache with the potential for providing a plurality of streams and the functional equivalent of streams as explained in the discussion of

Ramirez' teachings, earlier. The examiner would basically point out the determining is inherent in all the art since programs are not written as a series of streams. Also, inherently, to finally determine useful streams one must ultimately know the actual values which decide the direction of conditional branches, and this is known when the values are written-back/committed.

19. As to 14(b), when the basic blocks of the prior art consist of ISA-implementation specific instructions the instructions are certainly contiguous with basic blocks. Park taught a decoded instruction trace cache which would have all of its instructions as ISA-implementation specific instructions (col. 4, lines 3-6). Nair (Exploiting ...) taught VLIW-type instructions which has sub-instructions which are ISA-implementation specific instructions (Abstract). Ramirez teachings about trace caches of Pentium 4 micro-ops certainly taught ISA-implementation specific instruction contiguous with basic blocks. As to Nair (Patent No. 6,304,962), see paragraph 14, *supra*.

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

21. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

22. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
PRIMARY EXAMINER